REMARKS

35 U.S.C. Section 101 Rejections

Applicants have here in amended the specification to obviate the cited 35 USC section 101 rejection.

35 U.S.C. Section 112 Rejections

Claim 1 has been amended and claims 31 and 32 have been canceled to obviate the cited 35 USC section 112 rejection.

35 U.S.C. Section 102 Rejections

Paragraph 8 of the above referenced Office Action states that independent Claims 1, 11, and 21 are rejected under 35 USC section 102 as being anticipated by Devine (US Patent Number 6,397,242). Applicants have amended independent Claims 1, 11, and 21 to more particularly point out aspects of the present invention.

With respect to claim 1, Applicants have amended claim 1 to recite a method for supporting input/output for a virtual machine, comprising:

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executing virtual machine application instructions, wherein the application instructions are executed using micro architecture code of a processor architecture, wherein the micro architecture code includes an

> instruction interpreter to execute the virtual machine application
> instructions;
>> receiving an I/O access from the virtual machine application;
>> upon receiving the I/O access, generating an exception;
>> performing the I/O access by using a host operating system;
>> updating state data for the virtual machine application in
> accordance with the I/O access; and
>> resuming execution of the virtual machine application.

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As explicitly recited in claim 1, the micro architecture code of the processor architecture includes instruction interpreter to execute the virtual machine application instructions. Similar limitations are included in each of the independent claims 11 and 21.

Applicants have reviewed the Devine reference and assert that Devine does not show or suggest a micro architecture code instruction interpreter as in the claimed invention. Devine describes the operation of a virtual machine monitor, however, the detection of Devine (e.g., Devine col. 12 line 38) is not a micro architecture code instruction interpreter as in the claimed invention.

Because of this, Applicant asserts that the present invention as recited in the amended Claims 1-30 is not anticipated by Devine within the meaning of 35 USC Section 102.

With respect to dependent claims 2, 12 and 22, further limitations are added, wherein the instruction interpreter is further configured to function

with an instruction translator to translate target instructions into host VLIW instructions to execute the virtual machine application instructions. Applicant asserts that there is no disclosure or suggestion within Devine for any instruction translator operating in conjunction with an instruction interpreter to translate target instructions into host VLIW instructions.

With respect to dependent Claims 3, 13, and 23, further limitations are added, wherein the micro architecture code includes an instruction translator to execute the virtual machine application instructions. There is no disclosure of translation (e.g., from a host instruction set to a target instruction set) to run both the virtual machine monitor and the virtual machine as in the claimed invention.

With respect to dependent Claims 8, 18 and 28, further limitations are added, wherein the virtual machine application instructions comprise target instructions and the micro architecture code comprises host instructions. Applicants point out that the description of target instructions and host instructions are a particular result of the architecture of the processor of the claimed invention (e.g., utilizing an instruction interpreter and an instruction translator). Because of this, these limitation are not shown or suggested by the Devine reference.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
WAGNER, MURABITO & HAO

Dated: 10/12 , 2007

Glenn Barnes
Registration No. 42,293

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060